9-Line Multimode LVD/SE SCSI Terminator

The IMP5241/42 is a multimode SCSI terminator that conforms to the SCSI Parallel Interconnect-2 (SPI-2) specification developed by the T10 standards committee for low voltage differential (LVD) termination, while providing backwards compatibility to the SCSI, SCSI-2, and SPI single-ended specifications. Multimode compatibility permits the use of legacy devices on the bus without hardware alterations. Automatic mode selection is achieved through voltage detection on the diffsense line.

The IMP5241/42 utilizes IMP's adaptive non-linear technology for the ultimate in SCSI bus performance while saving component cost and board area. Elimination of the external capacitors also mitigates the need for a lengthy capacitor selection process. The individual high bandwidth drivers also maximize channel separation and reduce channel to channel noise and cross talk. The high bandwidth architecture insures ULTRA2 performance while providing a clear migration path to ULTRA3 and beyond.

When the IMP5241/42 is enabled, the differential sense (DIFFSENSE) pin supplies a voltage between 1.2V and 1.4V. In application, this pin is tied to the DIFFSENSE input of the corresponding LVD transceivers. This action enables the LVD transceiver function. DIFFSENSE is capable of supplying a maximum of 15mA. Tying the DIFFSENSE pin high places the IMP5241/42 in a HiZ state indicating the presence of an HVD device. Tying the pin low places the part in a single-ended mode while also signaling the multimode transceiver to operate in a single-ended mode.

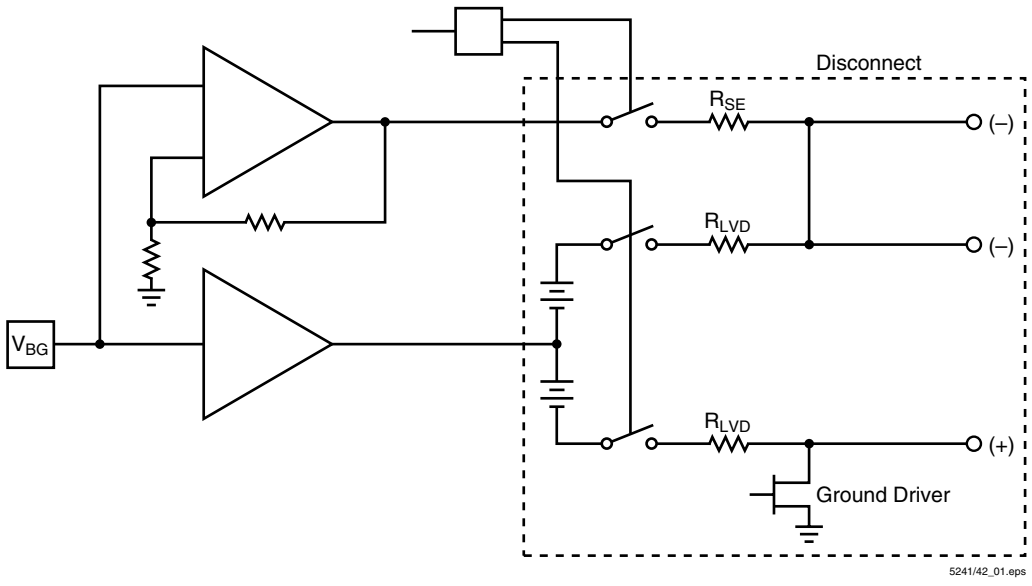
Recognizing the needs of portable and configurable peripherals, the IMP5241/42 have a TTL compatible sleep/disable mode. During this sleep/disable mode, power dissipation is reduced to a meager 5µA while also placing all outputs in a HiZ state. Also during sleep/disable mode, the DIFFSENSE function is disabled and is placed in a HiZ state.

Another key feature of the IMP5241/42 is the MASTER/$\overline{\text{SLAVE}}$ function. Driving this pin high or floating the pin enables the 1.3V DIFFSENSE reference. Driving the pin low disables the on board DIFFSENSE reference and enables use of an external master reference device.

Key Features

- Auto-selectable LVD or single-ended termination
- 3.0pF maximum disabled output capacitance
- Fast response, no external capacitors required
- Compatible with active negation drivers
- 5µA supply current in disconnect mode
- Logic command disconnects all termination lines
- DIFFSENSE line driver
- Ground driver integrated for single-ended operation
- Current limit and thermal protection
- Hot-swap compatible (single-ended)
- Compatible with SCSI 1, 2, 3, FAST-20, and the pending SPI-2 LVD
- See IMP5244/45 for LVD only termination

Block Diagram



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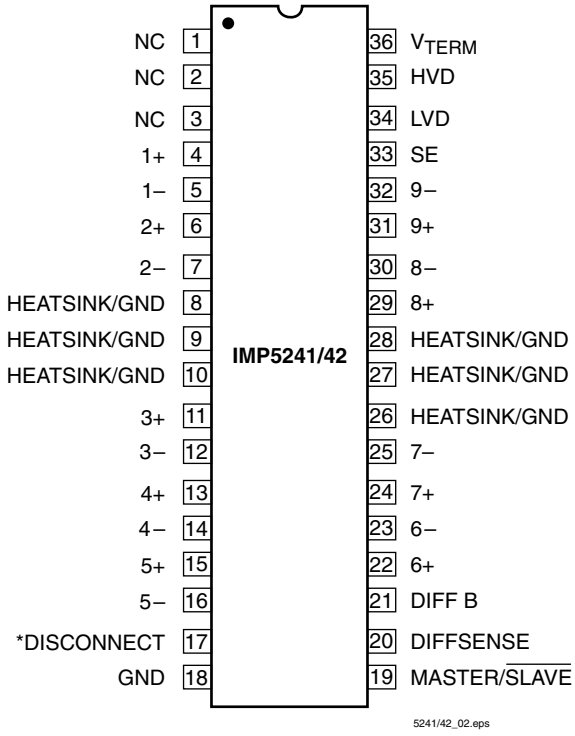
Pin Configuration

SSOP Package



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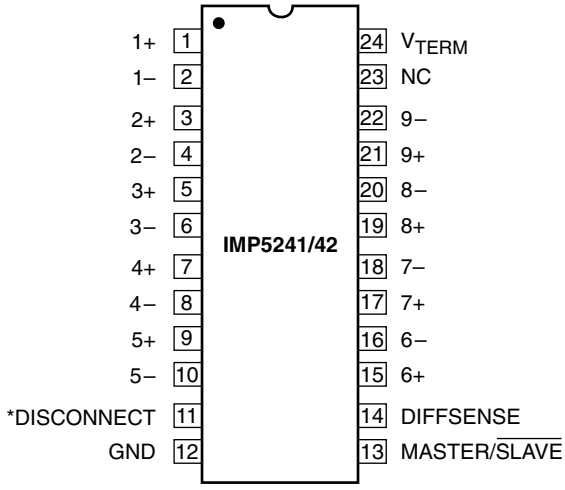
TSSOP Package



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$\overline{\text{DISCONNECT}}$ for the IMP5242

Ordering Information

Part Number	Temperature Range	Package
IMP5241CDB	0°C to 70°C	36-Pin Plastic SSOP
IMP5242CDB	0°C to 70°C	36-Pin Plastic SSOP
IMP5241CPW	0°C to 70°C	24-Pin Plastic TSSOP
IMP5242CPW	0°C to 70°C	24-Pin Plastic TSSOP

Note: All surface-mount packages are available in Tape & Reel. Append the letter "T" to part number. (i.e. IMP5241/42CDBT)

Absolute Maximum Ratings[1]

TermPwr Voltage . . . . . +7V
Operating Junction Temperature
Plastic (DB, PW Packages) . . . . . 150°C
Storage Temperature Range . . . . . –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) . . . . . 300°C

Note: 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

Thermal Data

DB Package:
Thermal Resistance Junction-to-Ambient, θ_{JA} . . . . . 50°C/W
PW Package:
Thermal Resistance Junction-to-Ambient, θ_{JA} . . . . . 100°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. No ambient airflow is assumed.

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Recommended Operating Conditions[2]

Parameter		Symbol	Min	Typ	Max	Units
Termpwr Voltage	LVD	V_{TERM}	3.0		5.25	V
	SE	V_{TERM}	3.5		5.25	V
Signal Line Voltage			0		5.0	V
Disconnect Input Voltage			0		V_{TERM}	V
Operating Virtual Junction Temperature Range — IMP5241/5242C			0		70	°C

Note: 2. Range over which the device is functional.

Electrical Characteristics

Unless otherwise specified, these specifications apply over the operating ambient temperature range of 0°C ≤ T_A ≤ 70°C. TermPwr = 4.75V. DISCONNECT: IMP5241 = LOW, $\overline{\text{DISCONNECT}}$: IMP5242 = HIGH. Low duty cycle pulse testing techniques are used which maintain junction and case temperatures equal to the ambient temperature.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
LVD Terminator Section						
TermPwr Supply Current	$LVDI_{CC}$	All terminator lines open		25	30	mA
		IMP5241: $\overline{\text{DISCONNECT}}$ > 2.0V IMP5242: $\overline{\text{DISCONNECT}}$ < 8.0V		15	35	µA
Common Mode Voltage	V_{CM}		1.125	1.25	1.375	V
Offset Voltage	V_{FSB}	Open circuit between – and + (see Note 3)	100	112	125	mV
Differential Terminator Impedance	Z_D	V_{OUT} differential = –1V to 1V	100	105	110	Ω
Common Mode Impedance	Z_{CM}	0V to 2.5V	100	200	300	Ω
Output Capacitance	C_O	IMP5241: $\overline{\text{DISCONNECT}}$ > 2.0V IMP5242: $\overline{\text{DISCONNECT}}$ < 8.0V		2.5		pF
Output Leakage	I_{LEAK}	IMP5241: $\overline{\text{DISCONNECT}}$ > 2.0V IMP5242: $\overline{\text{DISCONNECT}}$ < 8.0V V_{LINE} = 0 to 4V, T_A = 25°C			2	µA
		IMP5241: $\overline{\text{DISCONNECT}}$ > 2.0V IMP5242: $\overline{\text{DISCONNECT}}$ < 8.0V V_{TERM} = 0V, V_{LINE} = 2.7V		1		
Mode Change Delay	t_{DF}	DIFFSENSE = 1.4V to 0V		115		ms
DIFFSENSE Section						
DIFFSENSE Output Voltage	V_{DIFF}		1.2	1.3	1.4	V
DIFFSENSE Output Source Current	I_{DIFF}	V_{DIFF} = 0V	5.0		15.0	mA
DIFFSENSE Sink Current		V_{DIFF} = 2.75V			200	µA
DIFFSENSE Output Leakage		IMP5241: $\overline{\text{DISCONNECT}}$ > 2.0V IMP5242: $\overline{\text{DISCONNECT}}$ < 8.0V T_A = 25°C			10	µA
Single-Ended Terminator Section						
TermPwr Supply Current	SEI_{CC}	All terminator lines open, MASTER/$\overline{\text{SLAVE}}$ = 0V		9	10	mA
		All terminator lines 0.2V, MASTER/$\overline{\text{SLAVE}}$ = 0V		214	226	
		IMP5241: $\overline{\text{DISCONNECT}}$ > 2.0V IMP5242: $\overline{\text{DISCONNECT}}$ < 8.0V		15	35	µA
Terminator Output High Voltage			2.6	2.85		V
Output Current		V_{OUT} = 0.2V	21	23	24	mA

Note: 3. Open circuit failsafe voltage.

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Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Single-Ended Terminator Section (cont.)						
Sink Current		V_{OUT} = 4V, all lines	45	65		mA
Output Capacitance		IMP5241: $\overline{\text{DISCONNECT}}$ > 2.0V IMP5242: $\overline{\text{DISCONNECT}}$ < 8.0V		2.5		pF
Leakage Current		IMP5241: $\overline{\text{DISCONNECT}}$ > 2.0V IMP5242: $\overline{\text{DISCONNECT}}$ < 8.0V V_{OUT} = 0 to 4V, T_A = 25°C			2	µA
		IMP5241: $\overline{\text{DISCONNECT}}$ > 2.0V IMP5242: $\overline{\text{DISCONNECT}}$ < 8.0V V_{TERM} = Open, V_{LINE} = 2.7V		1		
Ground Driver Impedance	Z_G	I = 2mA			100	Ω
Thermal Shutdown				150		°C
DISCONNECT Section						
DISCONNECT Thresholds	V_{TH}		0.8		2.0	V
Input Current	I_{IL}	IMP5241: DISCONNECT = 0V			10	µA
	I_{IL}	IMP5242: $\overline{\text{DISCONNECT}}$ = 0V			100	nA
	I_{IM}	IMP5241: DISCONNECT = 4.75V			100	nA
	I_{IM}	IMP5242: $\overline{\text{DISCONNECT}}$ = 2.4V			10	µA
MASTER/$\overline{\text{SLAVE}}$ Section						
MASTER/$\overline{\text{SLAVE}}$ Thresholds			0.8		2.0	V
Input Current		MASTER/$\overline{\text{SLAVE}}$ = 0V			10	µA
		MASTER/$\overline{\text{SLAVE}}$ = 4.75V			100	nA

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Application Information

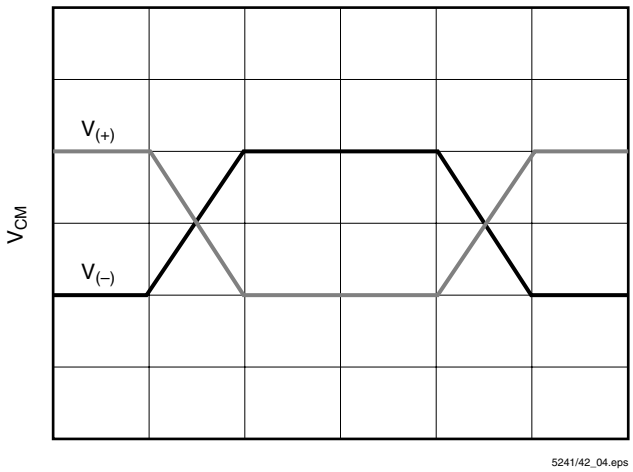

Figure 1. Bus Voltage

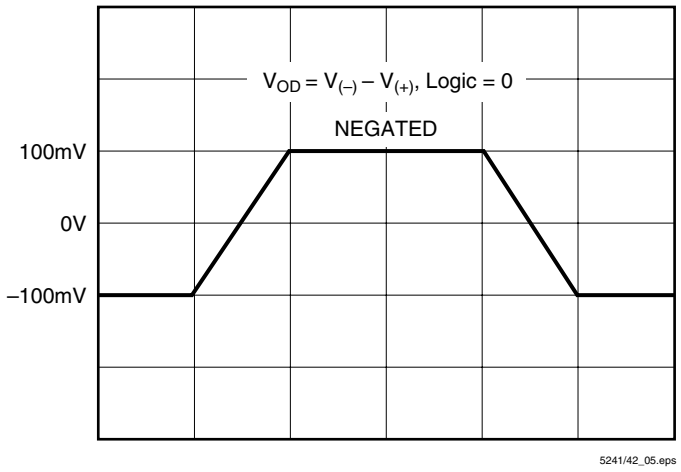

Figure 2. V_{OD}

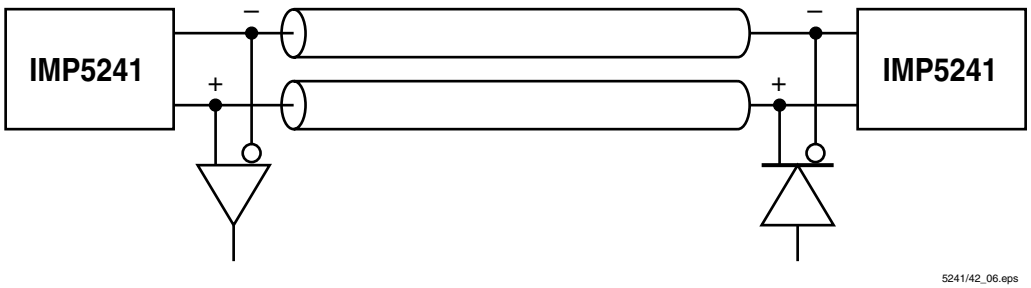

Figure 3.

Table 1. MASTER/$\overline{\text{SLAVE}}$ Function Table

MASTER/ $\overline{\text{SLAVE}}$	DIFFSENSE Status	Output Current
L*	HiZ	0mA
H	1.3V	15mA Source
Open (Pull-up)	1.3V	15mA Source

**When in the LOW state, the terminator will detect the DIFFSENS line state.*

Table 2. DIFFSENSE/Power Up/Power Down Function Table

IMP5241 DISCONNECT	IMP5242 $\overline{\text{DISCONNECT}}$	DIFFSENS	Outputs		Current
			Status	Type	
L	H	L < 0.5V	Enable	SE	7mA
L	H	0.7V to 1.9V	Enable	LVD	21mA
L	H	H > 2.4V	Disable	HiZ	1mA
H	L	X	Disable	HiZ	10µA
Open	Open	X	Disable	HiZ	10µA

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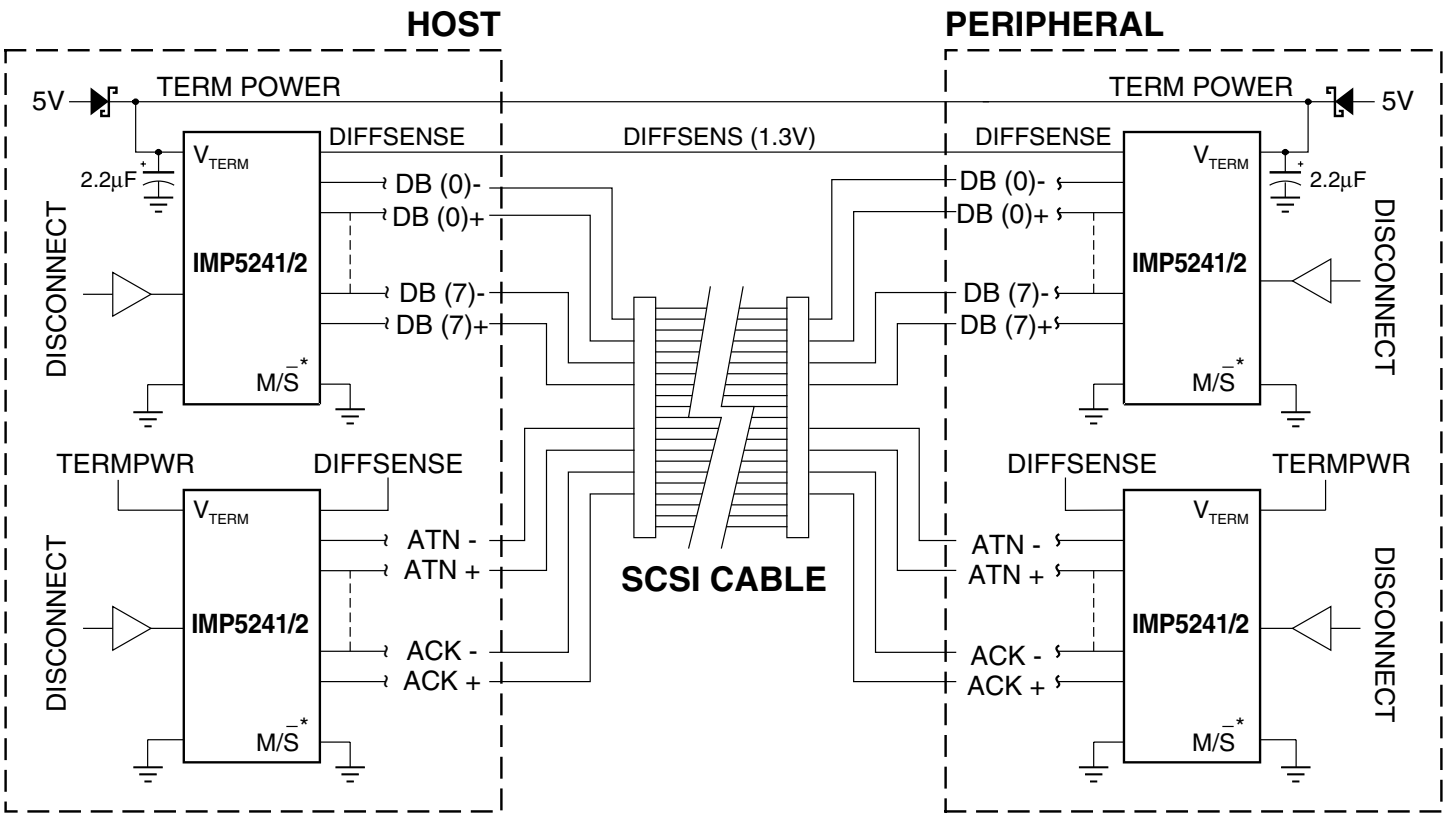
Application Information



Note: In Single-Ended operation, the + signals become ground. In SE mode the DIFFSENS line is < 0.5V.

* M/$\overline{S}$ = MASTER/$\overline{SLAVE}$.

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Figure 4. Application Schematic

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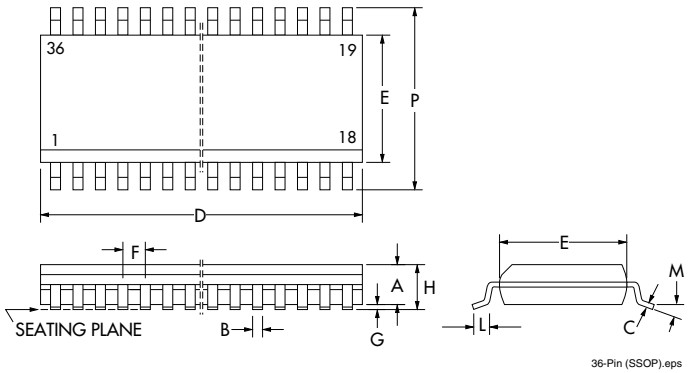
Package Dimensions

DB

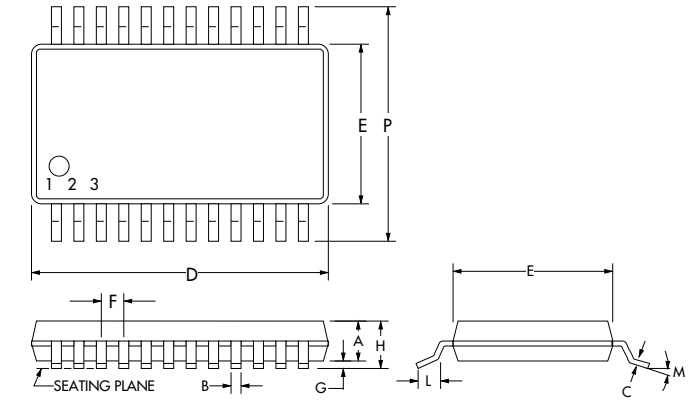
Plastic (SSOP) Widebody SOIC (36-Pin)



36-Pin (SSOP).eps

PWP

Thin Small Shrink Outline (TSSOP) (24-Pin)



24-Pin (TSSOP).eps

	Inches		Millimeters	
	Min	Max	Min	Max
Plastic (SSOP) Widebody SOIC (36-Pin)				
A	0.084	0.100	2.14	2.54
B	0.011	0.020	0.29	0.51
C	0.0091	0.0125	0.23	0.32
D	0.598	0.606	15.20	15.40
E	0.291	0.299	7.40	7.60
F	0.031 BSC		0.80 BSC	
G	0.004	0.012	0.10	0.30
H	0.096	0.104	2.44	2.64
L	0.016	0.050	0.40	1.27
M	0°	8°	0°	8°
P	0.398	0.414	10.11	10.51
*LC	–	0.004	–	0.10
Thin Small Shrink Outline (TSSOP) (24-Pin)				
A	.032	.041	0.80	1.05
B	0.007	0.012	0.19	0.30
C	0.0035	0.0079	0.09	0.20
D	0.303	0.311	7.70	7.90
E	0.169	0.176	4.30	4.5
F	0.025 BSC		0.65 BSC	
G	0.002	0.005	0.05	0.15
H	–	0.047	–	1.20
L	0.017	0.030	0.45	0.75
M	0°	8°	0°	8°
P	0.246	0.256	6.25	6.50
*LC	–	0.004	–	0.10

** Lead Coplanarity.*

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